Therefore isolators 6A and 6B have been used to isolate the bit line from the sensing nodes SA and SB associated with the sense amplifier. The isolators are devices which completely isolate the bit lines from the sense nodes.

As noted earlier, while the aforenoted device was successful in isolating the bit lines from the sense nodes, thus eliminating the requirement to charge the bit line capacitances 5A and 5B during the initial part of the sensing interval, the differential between sense nodes was sometimes uncertain and sometimes small, and was affected by noise, or even being below the noise level. Accordingly an incorrect bit value could be sensed.

In addition, since the isolator must be turned on and off, additional steps in the memory access sequence must be performed. Further, the isolator must be inhibited in order to restore the logic level to the memory capacitor and indeed, if an incorrect bit were read, the restored bit value would also be incorrect. Clearly both speed and reliability of the memory were sacrificed.

FIG. 2 illustrates an embodiment of the present invention. An imperfect isolation device 8A and 8B, driven from a source ϕ_{In} is connected in series between each bit line and each sense node. In the embodiment shown in FIG. 2 the imperfect isolation devices are N-channel enhancement mode FETs 8A and 8B. However alternatively, or in addition, P-channel enhancement mode FETs are connected in series between each bit line and each sense node. The gates of the transistors 9A and 9B are connected together to a logic source ϕ_{Ip}.

With reference to FIGS. 2 and 3, operation of the device is as follows. At the beginning of an active cycle the voltage ϕ_{IN} is brought from a boosted level, e.g. V_{pp} to a lower level that still allows cell charge to flow to the sense amplifier as noted, e.g. V_{dd}. Then, as described earlier, either transistor 2A or 2B is enabled, causing the charge on either bit storage capacitor 1A or 1B to be dumped on an associated bit line. Charge on the bit line leaks through the high resistance source-drain circuit transistor 8A or 8B (assuming transistors 9A and 9B are not present) to the sense node SA or SB, charging the small capacitance associated therewith.

Subsequently the sense amplifier 3 is enabled by applying high logic level ϕ_s and low logic level $/\phi_R$, as described earlier. The sense amplifier is caused to apply the full logic levels ϕ_s and $/\phi_R$ to the sense nodes SA and SB, latching due to the differential thereacross. However due to the voltage drop between the sources and drains of transistors 8A and 8B, bit line capacitances 5A and 5B will only be charged up to a reduced voltage less than full logic level applied to the sense nodes. Since capacitances 5A and 5B are charged a reduced amount, the sensing interval is considerably reduced from the prior art; the sensing is faster because the sense node voltage differential develops faster for the same sense current budget. Data can be read out over the data bus by enabling column access transistors 4A and 4B, as soon as a sufficient potential exists across the sense nodes. Hence memory access time is improved by the isolation devices. While the restore charge on capacitors 1A and 1B is less than full logic level, they can be fully restored after column access.

After the peak current has occurred in the first stage of sensing the ϕ_{IN} level is brought back up to the boosted level V_{pp} to allow full restore of the bit lines. This causes a second peak in sensing current. Compared to prior art sensing current peaks are lower and are distributed over time.

It was noted earlier that P-channel transistors 9A and 9B could be used in place of transistors 8A and 8B, or in series therewith as shown in the figure. If P-channel transistors are used, their gates should initially be at a ϕ_{IP} level V_{bb}, and are raised to a level V_{ss} during the initial part of sensing when a high impedance isolation device is required.

It had been noted earlier that resistive voltage drops in the conductive tracks in the semiconductor memory from the sense amplifier driver circuits to the far end of the array cause quick sensing at the near end of the array (close to the sense amplifier driver circuits) and slow (retarded) sensing at the far end of the array. Thus memory access must be delayed to accommodate the sensing of the slowest column.

According to another embodiment of the invention, rather than driving the logic $/\phi_s$ and ϕ_R input leads of the sense amplifiers directly from the sense amplifier drivers, local pull down FETs or pull up FETs are used. Indeed, these FETs may be shared among several sense amplifiers in adjacent columns.

As shown in FIG. 2, rather than the sense amplifier being connected to $/\phi_s$ and ϕ_R logic sources, they are connected through the source-drain circuits of FETs 12A and 12B to voltage sources V_{dd} and ground (V_{ss}) respectively. The gates of transistors 12A and 12B are driven from the $/\phi_R$ and ϕ_s logic sources respectively.

The ground and V_{dd} power tracks on an integrated circuit memory normally are of low resistance. Therefore the provision of those sources to the sense amplifiers is through short and low resistance conductors.

However since the $/\phi_R$ and ϕ_s logic signals driving the gates of transistors 12A and 12B require only a small amount of current, there will be a considerably reduced voltage drop in their conductive tracks from one end of the memory to the other. Thus the difference in operation time of the sense amplifiers between the near and far ends is considerably reduced, and can be considerably increased in speed over prior art DRAMs.

The result of the last-described embodiment is increased reliability, since leaky bit lines which have been deprogrammed will not affect sense line current in other bit lines, if local sense clock drivers are shared only among bit lines with the same redundancy address. No additional power supplies are required other than those normally on the chip.

The result of the above embodiments is increase in sensing speed and more uniformity of sensing speed across a large DRAM.

It should be noted that either of the embodiments can be used separately or in conjunction. For example, N-channel bit line isolation devices could be used in conjunction with local sensing amplifier enabling pull downs as described, to control peak V_{dd} current and V_{ss} current respectively.

A person understanding this invention may now conceive of alternative structures and embodiments or variations of the above. All of those which fall within the scope of the claims appended hereto are considered to be part of the present invention.

We claim:

1. A dynamic random access memory (DRAM) comprising:

(a) a plurality of bit storage capacitors,

(b) a folded bit line comprised of a complementary bit line pair for receiving charge stored on one of said capacitors, having bit line capacitance,

(c) a sense amplifier having a pair of sense nodes for sensing a voltage differential across said sense nodes,

(d) high resistance controllable current leakage imperfect isolating means connecting said bit line to said sense nodes for receiving an enabling voltage for causing current leakage therethrough between said sense nodes and the bit line while maintaining high resistance,

(e) means for applying said enabling voltage for causing effective current to leak through the imperfect isolating means,

(f) means for enabling said sense amplifier and establishing full predetermined logic levels across said sense nodes,

(g) means for disabling said imperfect isolating means and thereby removing isolation between said sense nodes and the bit line,

whereby current passing through the sense amplifier to said sense nodes is enabled to charge said bit line capacitance through said imperfect isolating means to a predetermined logic voltage level.

2. A DRAM as defined in claim 1 in which said imperfect isolating means is a pair of N-channel enhancement mode field effect transistors each having a source-drain circuit in series with a bit line of the bit line pair.

3. A DRAM as defined in claim 2 including a voltage source applied to gates of each field effect transistor having an initial voltage level which is higher than said logic voltage level and a following enabling voltage level which is equal to said logic level, and at a later time a disabling voltage equal to the initial voltage level.

4. A DRAM as defined in claim 1 in which said isolating means is a pair of P-channel enhancement mode field effect transistors each having a source-drain circuit in series with a bit line of the bit line pair.

5. A DRAM as defined in claim 4 including a voltage source applied to gates of each field effect transistor having an initial voltage level which is lower than said logic voltage level and a following enabling voltage level which is equal to said logic level, and at a later time a disabling voltage equal to said initial voltage level.

6. A dynamic random access memory (DRAM) as defined in claim 1, further comprising:

(a) the sense amplifier having respective sense enable and restore enable inputs for providing full high and full low logic levels respectively to said sense nodes,

(b) power supply means for providing full high and full low logic level voltages,

(c) a pair of field effect transistors, one being a P-channel enhancement mode type having its source-drain circuit connected between said restore enable input and the high logic level power supply voltage and the other being an N-channel enhancement mode type having its source-drain circuit connected between the sense enable input and the low logic level power supply voltage, and

(d) means for providing restore and sense signals to gates of said one and other field effect transistors respectively,

whereby restore and sense current is supplied to said sense amplifier from said power supply means rather than from said means for providing restore and sense signals.

7. A dynamic random access memory (DRAM) as defined in claim 1 comprising a plurality of bit lines and

associated sense amplifiers, the bit lines being arrayed across an integrated circuit chip and the sense amplifiers being disposed in a row, a pair of low-resistance power supply conductors extending in parallel with said row for carrying logic high level and logic low level voltages, sense amplifier enabling signal conductors extending across said chip accessible to said sense amplifiers, means for coupling sense inputs of said sense amplifiers to said power supply conductors, and means coupling said sense amplifier enabling signal conductors to enabling inputs of said means for coupling sense inputs, for enabling passage of current resulting from said logic high level and low level voltages to said sense amplifiers.

8. A DRAM as defined in claim 7 in which said means for coupling sense inputs of said sense amplifiers is comprised of field effect transistors having their gates connected to said sense amplifier enabling signal conductors, said gates forming said enabling inputs.

9. A DRAM as defined in claim 8 in which the sense inputs of groups of said sense amplifiers are connected together to the same field effect transistor drain terminal.

10. A DRAM as defined in claim 1, further comprising:

(a) the sense amplifier having sense enable and restore enable inputs for providing full high and full low logic levels respectively to said sense nodes,

(b) power supply means for providing full high and full low logic level voltages,

(c) a pair of field effect transistors, one having its source-drain circuit connected between said restore enable input and the high logic level power supply voltage and the other having its source-drain circuit connected between the sense enable input and the low logic level power supply voltage, and

(d) means for providing restore and sense signals to gates of said one and other field effect transistors respectively,

whereby restore and sense current is supplied to said sense amplifier from said power supply means rather than from said means for providing restore and sense signals.

11. A DRAM as defined in claim 1, further comprising a plurality of bit lines and associated sense amplifiers, the bit lines being arrayed across an integrated circuit chip and the sense amplifiers being disposed in a row, a pair of low-resistance power supply conductors extending in parallel with said row for carrying logic high level and logic low level voltages, sense amplifier enabling signal conductors extending across said chip accessible to said sense amplifiers, means for coupling sense inputs of said sense amplifiers to said power supply conductors, and means coupling said sense amplifier enabling signal conductors to enabling inputs of said means for coupling sense inputs, for enabling passage of current resulting from said logic high level and low level voltages to said sense amplifiers.

12. A DRAM as defined in claim 3, further comprising a plurality of bit lines and associated sense amplifiers, the bit lines being arrayed across an integrated circuit chip and the sense amplifiers being disposed in a row, a pair of low-resistance power supply conductors extending in parallel with said row for carrying logic high level and logic low level voltages, sense amplifier enabling signal conductors extending across said chip accessible to said sense amplifiers, means for coupling

sense inputs of said sense amplifiers to said power supply conductors, and means coupling said sense amplifier enabling signal conductors to enabling inputs of said means for coupling sense inputs, for enabling passage of current resulting from said logic high level and low level voltages to said sense amplifiers.

13. A DRAM as defined in claim 5, further comprising a plurality of bit lines and associated sense amplifiers, the bit lines being arrayed across an integrated circuit chip and the sense amplifiers being disposed in a row, a pair of low-resistance power supply conductors extending in parallel with said row for carrying logic high level and logic low level voltages, sense amplifier enabling signal conductors extending across said chip accessible to said sense amplifiers, means for coupling sense inputs of said sense amplifiers to said power supply conductors, and means coupling said sense amplifier enabling signal conductors to enabling inputs of said means for coupling sense inputs, for enabling passage of current resulting from said logic high level and low level voltages to said sense amplifiers.

14. A DRAM as defined in claim 11 in which said means for coupling sense inputs of said sense amplifiers is comprised of field effect transistors having their gates connected to said sense amplifier enabling signal conductors, said gates forming said enabling inputs.

15. A DRAM as defined in claim 14 in which the sense inputs of groups of said sense amplifiers are connected together to the same field effect transistor drain terminal.

16. A method of sensing in a folded bit line type of dynamic random access memory (DRAM) having a bit

storage capacitor for coupling to the bit line and a sensing amplifier having sense nodes, comprising:

(a) imperfectly isolating the sense nodes of the sensing amplifier from the bit line using an imperfect isolating means,

(b) coupling the capacitor to the bit line, thereby dumping its charge thereon,

(c) leaking said charge through the imperfect isolating means to one of the sense nodes, thereby causing a voltage differential across said sense nodes,

(d) sensing said differential by said sense amplifier and applying full high and low logic voltage levels respectively to said sense nodes,

(e) inhibiting isolation of said sense nodes from said bit line, whereby full logic levels are applied to complementary bit lines of said folded bit line.

17. A method as defined in claim 16, in which the isolating means is comprised of the source-drain circuits of a pair of enhancement mode field effect transistors respectively connected between the sense nodes and the complementary bit lines of the folded bit line, and said isolating step is comprised of applying an inhibiting voltage to gates of said field effect transistors, and the inhibiting isolating step is comprised of changing the inhibiting voltage to the same voltage as one of said full logic voltage levels, whereby upon application of said full logic levels to said sense nodes during the sensing step, a field effect transistor having a gate voltage closest to a logic level applied to a sense node to which it is connected is caused to inhibit current flow into the bit line.

* * * * *

18. A method of sensing and restoring data stored in a dynamic random access memory (DRAM) comprising the steps of:

(a) applying a V_{dd} voltage to controlling inputs of a pair of bit line isolation devices coupled between a complementary bit line pair and a bit line sense amplifier;

(b) enabling an access transistor coupled between a bit storage capacitor and a bit line of the complementary bit line pair to dump charge from the bit storage capacitor to the bit line;

(c) enabling the bit line sense amplifier to sense a voltage differential created across the complementary bit line pair as a result of dumping charge from the bit storage capacitor;

(d) enabling a pair of column access devices coupled to the complementary bit line pair once the voltage differential has reached a sufficient value;

(e) applying a V_{pp} voltage higher than the V_{dd} voltage to the controlling inputs of the bit line isolation devices to allow full restore of the bit lines.

19. A method as claimed in claim 18 wherein the bit line isolation devices are N-channel field effect transistors (FETs).

20. A method as claimed in claim 18 wherein the step of enabling the bit line sense amplifier is comprised of applying an active high logic level and an active low logic level to inputs of the bit line sense amplifier.

21. A method is claimed in claim 20 wherein the active high logic level and active low logic level are applied to inputs of the bit line sense amplifier through local transistors connected to voltage source power tracks and gated by logic signals.

22. A method of sensing and restoring data stored in a dynamic random access memory (DRAM) comprising the steps of:

(a) applying a V_{dd} voltage to controlling inputs of a pair of bit line isolation devices coupled between a complementary bit line pair and a bit line sense amplifier;

(b) enabling an access transistor coupled between a bit storage capacitor and a bit line of the complementary bit line pair to dump charge from the bit storage capacitor to the bit line;

(c) enabling the bit line sense amplifier to sense a voltage differential created across the complementary bit line pair as a result of dumping charge from the bit storage capacitor;

(d) applying a V_{pp} voltage higher than the V_{dd} voltage to the controlling inputs of the bit line isolation devices to allow full restore of the bit lines.

23. A method as claimed in claim 22 wherein the bit line isolation devices are N-channel field effect transistors (FETs).

24. A method as claimed in claim 22 wherein the step of enabling the bit line sense amplifier is comprised of applying an active high logic level and an active low

logic level to inputs of the bit line sense amplifier.

25. A method is claimed in claim 7 wherein the active high logic level and active low logic level are applied to inputs of the bit line sense amplifier through local transistors connected to voltage source power tracks and gated by logic signals.